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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,504	02/29/2000	NORIMITSU SAKO	105393	1188

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[REDACTED] EXAMINER

YE, LIN

ART UNIT	PAPER NUMBER
2612	8

DATE MAILED: 09/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/515,504	SAKO, NORIMITSU
Examiner	Art Unit	
Lin Ye	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 February 2000.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-28 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1.) Certified copies of the priority documents have been received.
 2.) Certified copies of the priority documents have been received in Application No. _____.
 3.) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5_6. 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Umeda et al. U.S. Patent 6,452,632.

Referring to claim 1, the Umeda reference discloses in Figures 20A-B and 90, a CMOS image sensor (see Col. 14, lines 44-54), comprising: pixel sensors arranged in a two-dimensional array (in Figure 90); means, disposed in each pixel sensor, for obtaining a signal whose reset noise is reduced and that corresponds to the absolute value of the amount of incident light (see Col. 28, lines 29-35 and Col. 29, lines 60-65); and means for outputting said signal in a block-scanning fashion as shown in Figures 20A-B (See Col. 15, lines 1-15).

3. Claims 2-3 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee U.S. Patent 6,549,234.

Referring to claim 2, the Lee reference discloses in Figures 3-4, A pixel sensor for use in a CMOS image sensor, said pixel sensor comprising: a photodiode at a signal detection node; and a pair of pass transistors (See Figure 4, transistors NM42 and NM43), which passes a photodiode reset signal to the gate of a transistor (NM44) that resets said photodiode, only when said pixel sensor is selected (by column reset selection decoder 30 and line reset selection decoder 20).

Referring to claim 3, the Lee reference discloses pixel sensors being arranged in a two-dimensional array, wherein said photodiode reset signal is given as the logical AND (both on) of a column block selection signal (column reset signal CRS) and a pixel reset signal (line reset signal LRS) (See Col. 4, lines 45-51).

Referring to claim 6, the Lee reference discloses in Figures 3-4, a CMOS image sensor plurality of photogate-type pixel sensors arranged in a two-dimensional array; a pair of pass transistors (NM42 and NM43) for passing a photo gate control signal (from a predetermined poison in a pixel sensor structure Pxji) thereby transferring a signal charge, only when a corresponding row is selected; and a pair of pass transistors for passing a pixel transfer signal thereby allowing a signal charge to be transferred, only when a corresponding column block is selected (et. Unlike the CCD image sensor, CMOS image sensor cal allows arbitrary pixels to be read out).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11, 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda et al. U.S. Patent 6,452,632 in view of Arai et al. U.S. Patent 5,128,769.

Referring to claims 11, 17 and 23, The Umeda reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly state automatically adjusting the gain, focus and detecting substantial change in an image based on a several blocks in a central area of said CMOS image sensor.

The Arai reference discloses in Figures 1-2 and 10, a video camera includes an image sensor (2) of CCD or MOS type for estimating the average brightness over an entire screen of said image sensor from brightness detected for a several blocks in a central area (See Figure 2, central area 23A) and in a peripheral area of the screen (23B) (See Col. 5, lines 49-60 and Col. 6, lines 1-20); and a programmable gain amplifier (variable gain amplifier 64) having a gain that is automatically controlled in accordance with the estimated brightness (See Figure 10 and Col. 15, lines 44-55); detecting whether there is a substantial change in an image by reading several blocks in a central area and in peripheral area of an image screen of the image sensor; means for continuously taking an image over the entire screen when a substantial change is detected (See Col. 14, lines 61-68 and Col. 15, lines 1-4); adjusting focus by reading several blocks in a central area of an image screen of said CMOS image sensor; and means for taking an image over the entire screen after completion of the focus adjustment (See Col. 9, lines 7-18). The Arai reference is evidence that one of ordinary skill in the art at the time to see more advantages the video camera system can perform center area

weighted measuring mode to obtain a proper exposure, focus adjustment and suppress an unstable change in the exposure amount for a principal subject (as center area of image) caused by a motion of the principal subject or the video camera. For that reason, it would have been obvious to the camera device can perform automatically adjusting the gain, focus and detecting substantial change in an image based on a several blocks in a central area of said CMOS image sensor disclosed by Umeda.

6. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Umeda et al. U.S. Patent 6,452,632.

Referring to claim 8, The Lee reference discloses all subject matter as discussed in respected claims 2, except the reference does not explicitly show means for selectively connecting the output of the pixel sensor to a circuit for reading one row of block.

The Umeda reference discloses in Figures 20A-B and 90, a CMOS image sensor (see Col. 14, lines 44-54), comprising a pixel sensor; and means for selectively connecting the output of the pixel sensor to a circuit for reading one row of block. The Umeda reference is evidence that one of ordinary skill in the art at the time to see more advantages the CMOS type image sensor can be designed to selectively activate horizontal and vertical scanning lines to allow arbitrary pixels to be read out. For that reason, it would have been obvious to the CMOS image sensor has means for selectively connecting the output of the pixel sensor to a circuit for reading one row of block disclosed by Lee.

Referring to claim 10, the Lee and Umeda references disclose all subject matter as discussed with respected to same comment as with claim 8.

7. Claims 12, 14, 18, 20, 24 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Arai et al. U.S. Patent 5,128,769.

Referring to claims 12, 18 and 24, the Lee and Arai references disclose all subject matter as discussed with respect to same comment as with claims 11, 17 and 23.

Referring to claims 14, 20 and 26, the Lee and Arai references disclose all subject matter as discussed with respect to same comment as with claims 11, 17 and 23.

8. Claims 16, 22 and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Umeda et al. U.S. Patent 6,452,632 and Arai et al. U.S. Patent 5,128,769.

Referring to claims 16, 22 and 28, the Lee, Umeda and Arai references disclose all subject matter as discussed with respect to same comment as with claims 11, 17 and 23.

9. Claims 4-5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Pain et al. U.S. Patent 6,326,230.

Referring to claim 4, The Lee reference discloses all subject matter as discussed in respected claims 2, except the reference does not explicitly show the structure diagram of the CMOS sensor including floating diffusion at a signal detection node instead of the circuit diagram of CMOS sensor.

The Pain reference discloses in Figure 2A, a CMOS image sensor including a photoactive region (60) and floating diffusion (66) at a signal detection node. The Pain reference is

evidence that one of ordinary skill in the art at the time to see more advantages to use the floating diffusion to temporarily store the charges from the photoactive region to prevent the any loss image information before transfer to outside circuit. For that reason, it would have been obvious to the CMOS sensor including floating diffusion at a signal detection node disclosed by Lee.

Referring to claim 5, the Lee discloses wherein said transfer signal (read out signal) is given as the logical AND of column block selection signal (from column reset selection decoder) and a pixel transfer signal (row selection decoder).

Referring to claim 7, The Lee reference discloses all subject matter as discussed in respected claims 6, except the reference does not explicitly show wherein said pixel transfer signal falls down before said photogate control signal rises up.

The Pain reference discloses in Figure 3D, a pixel transfer signal (TX) falls down before the photogate control signal (PG) rises up. The Pain reference is evidence that one of ordinary skill in the art at the time to see more advantages photogate control signal rises up after the pixel transfer signal falls to prevent any charge from flowing back into sense nodes (See Col. 6, lines 8-13). For that reason, it would have been obvious to the CMOS sensor including means for pixel transfer signal falls down before said photogate control signal rises up disclosed by Lee.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Pain et al. U.S. Patent 6,326,230 and Umeda et al. U.S. Patent 6,452,632.

Referring to claim 9, the Lee, Pain and Umeda references disclose all subject matter as discussed with respect to same comment as with claim 8.

11. Claims 13, 15, 19, 21, 25 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent 6,549,234 in view of Pain et al. U.S. Patent 6,326,230 and Arai et al. U.S. Patent 5,128,769.

Referring to claims 13, 19 and 25, the Lee, Pain and Arai references disclose all subject matter as discussed with respect to same comment as with claims 11, 17 and 23.

Referring to claims 15, 21 and 27, the Lee, Pain and Arai references disclose all subject matter as discussed with respect to same comment as with claims 11, 17 and 23.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Roberts U.S 5,452,004 discloses the image device includes provision for random access of each image element or group of image elements in the array.
- b. Yadid-Pecht et al. U.S 6,175,383 discloses a method for controlling a sensor to reduce reset noise.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (703) 305-3250. If attempts to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

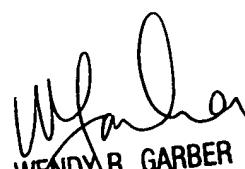
Commissioner of Patents and Trademarks
Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.



WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Lin Ye
September 4, 2003